Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. MR**
2. **Q0**
3. **D0**
4. **D1**
5. **Q1**
6. **D2**
7. **Q2**
8. **GND**
9. **CP**
10. **Q3**
11. **D3**
12. **Q4**
13. **D4**
14. **D5**
15. **Q5**
16. **VCC**

**.063”**

**.070”**

**10 9 8 7**

**6**

**5**

**4**

**3**

**15 16 1 2**

**11**

**12**

**13**

**14**

**MASK**

**REP**

**13625**

**D**

**HCT**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .007” X .007”**

**Backside Potential:**

**Mask Ref: 13625 D**

**APPROVED BY: DK DIE SIZE .063” X .070” DATE: 3/27/17**

**MFG: HARRIS - RCA THICKNESS .000” P/N: 54HCT174**

**DG 10.1.2**

#### Rev B, 7/1